Fig 1 (Prior Art)

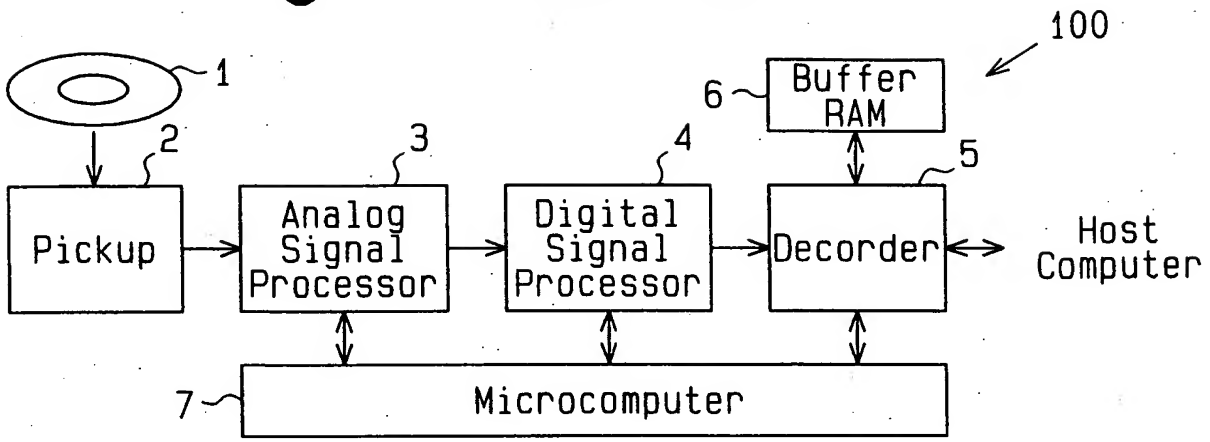

Fig.2 (Prior Art)

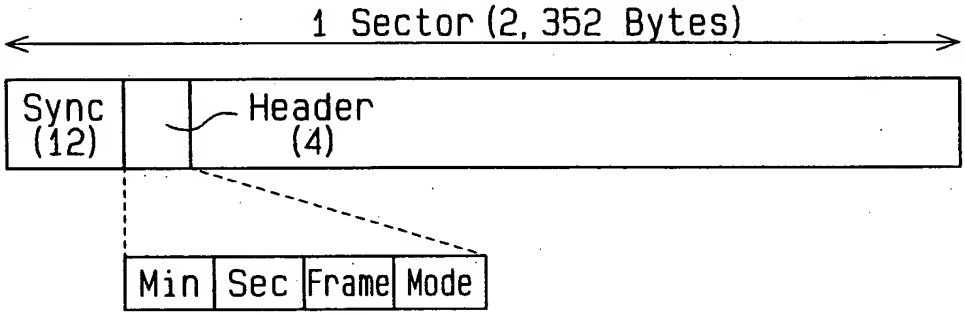

Fig.3 (Prior Art)

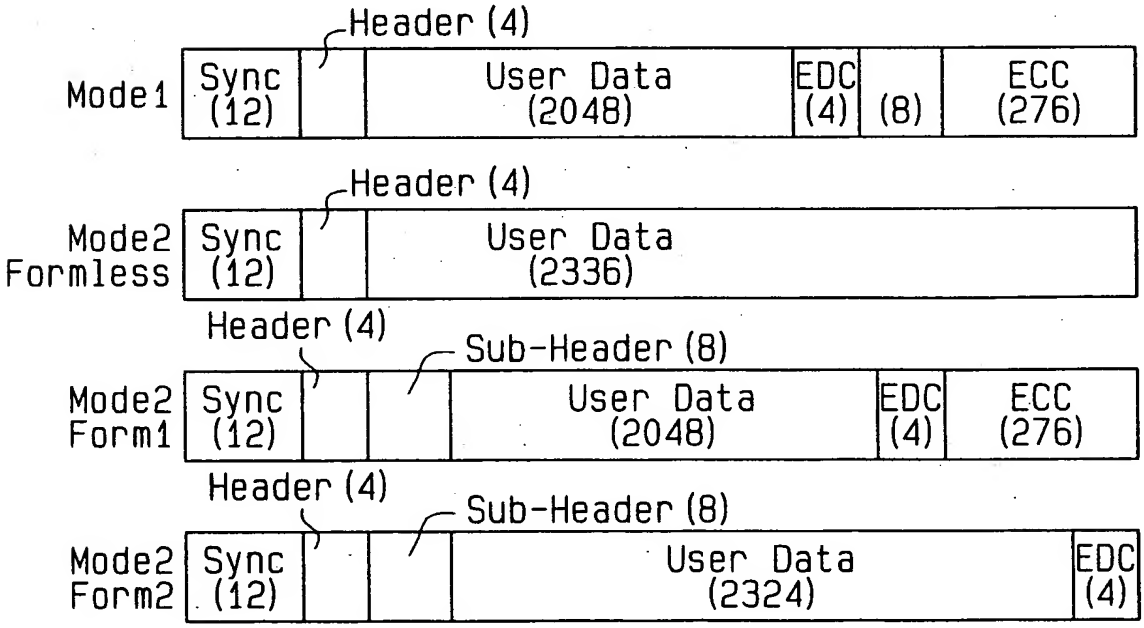

Fig.4A

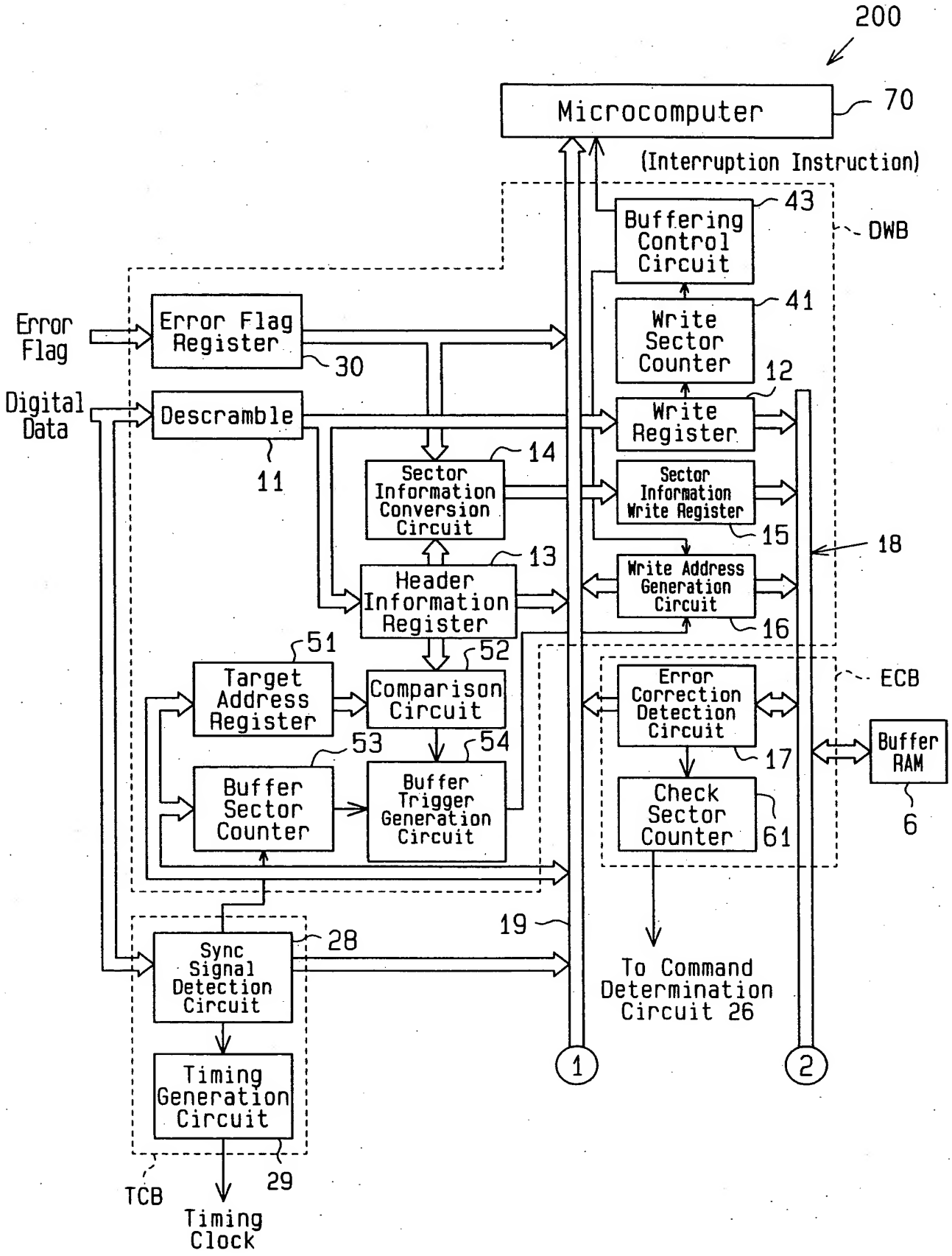
200
Microcomputer
70
(Interruption Instruction)
DWB
43
Buffering Control Circuit
41
Write Sector Counter
12
Write Register
Sector Information Write Register
15
18
Write Address Generation Circuit
16
ECB
Error Correction Detection Circuit
17
Check Sector Counter
61
Buffer RAM
6
To Command Determination Circuit 26
19
1
2
Error Flag
Error Flag Register
30
Digital Data
Descramble
11
14
Sector Information Conversion Circuit
13
Header Information Register
51
Target Address Register
52
Comparison Circuit
53
Buffer Sector Counter
54
Buffer Trigger Generation Circuit
28
Sync Signal Detection Circuit
Timing Generation Circuit
29
TCB
Timing Clock

Fig.4B

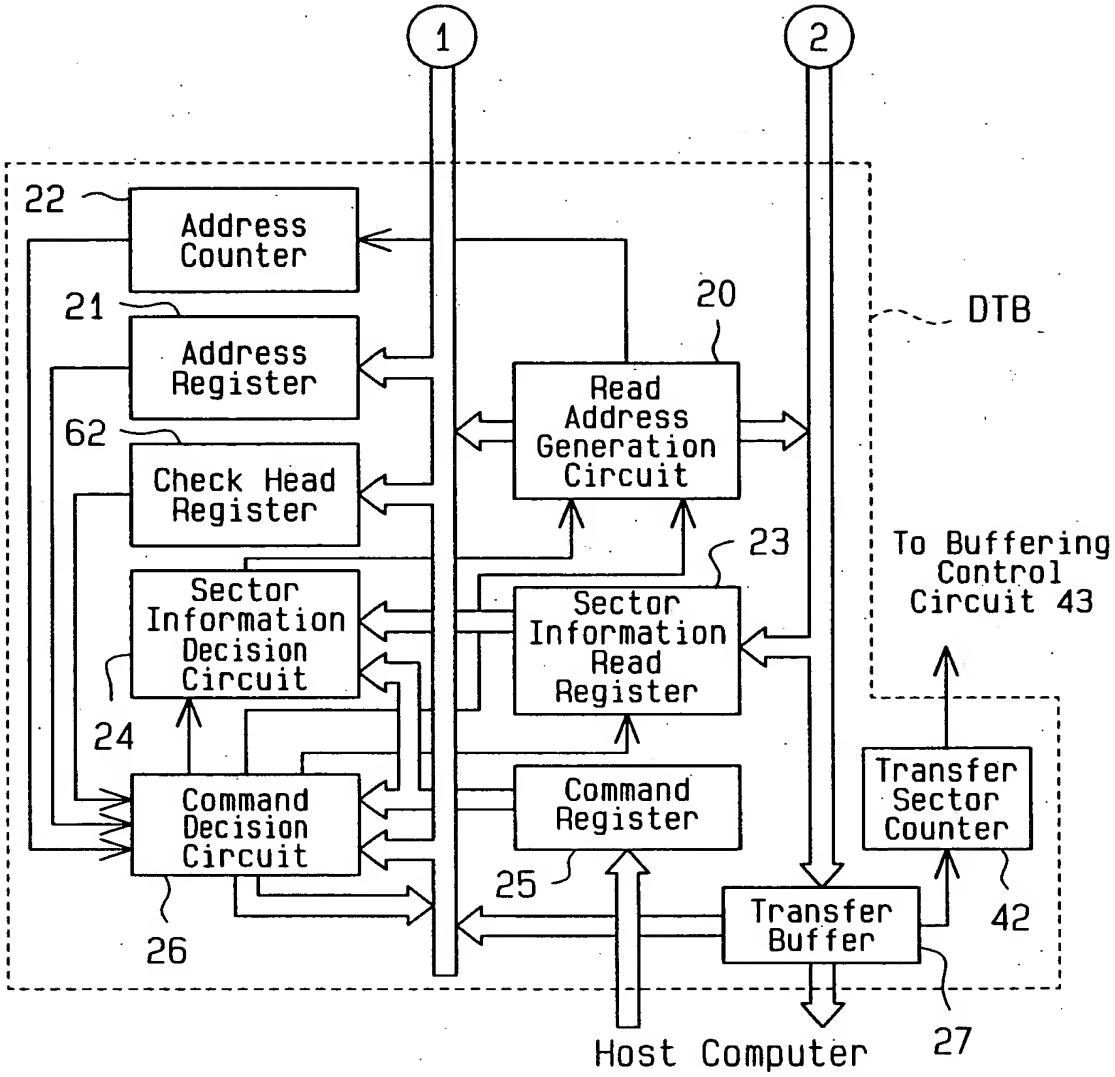
1
2
22
Address Counter
21
Address Register
62
Check Head Register
Sector Information Decision Circuit
24
Command Decision Circuit
26
20
Read Address Generation Circuit
23
Sector Information Read Register
Command Register
25
Transfer Buffer
27
Host Computer
DTB
To Buffering Control Circuit 43
Transfer Sector Counter
42

Fig 5

Format	Sector Information
Mode0	000b
Mode1	010b
Mode2Formless	011b
Mode2Form1	100b
Mode2Form2	101b
Other	111b

Fig.6

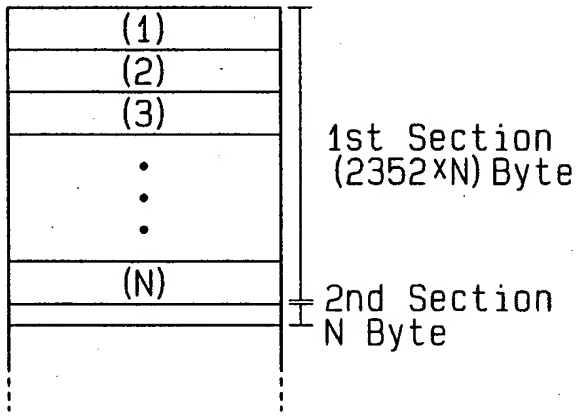

Fig.7

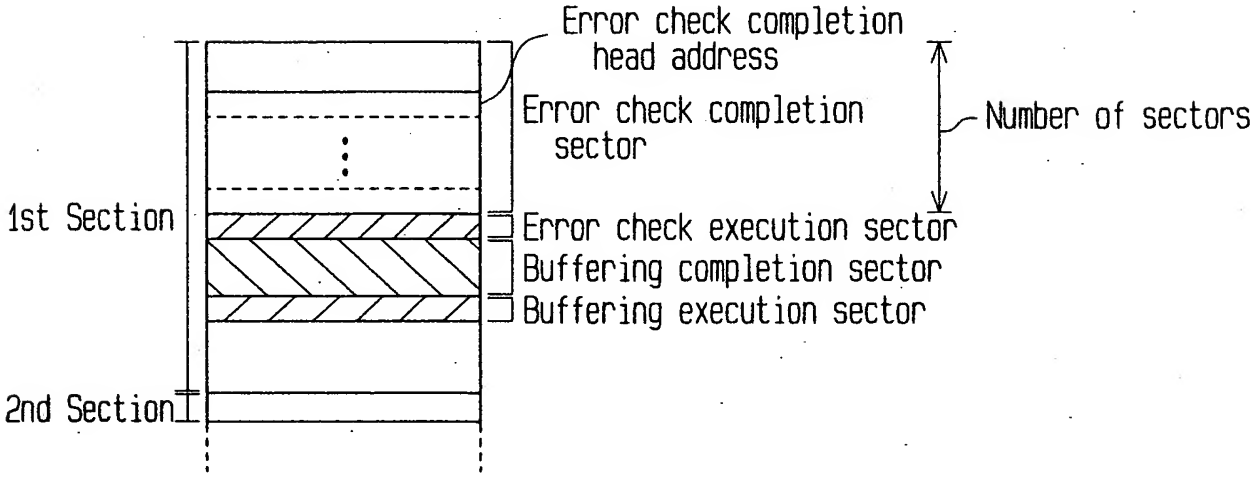

Fig.8

Transfer Request Command

byte \ bit	7	6	5	4	3	2	1	0
0	Operation code							
1	000b			000b, 010b, 011b, 100b, 101b Flag Bit			0	0
2	00h							
3	LBA (Logic Address)							
4								
5								
6	TBL (Transfer Block Number)							
7								
8								
9	10h, B0h, B8h, F0h, F8h							
10	00h							
11	00h							

Fig.9